STB50N25M5

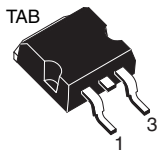
N-channel 250 V, 0.065 Ω, 28 A, MDmesh™ V Power MOSFET in D²PAK package

Datasheet — production data

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STB50N25M5	250 V	< 0.075 Ω	28 A

- Amongst the best $R_{DS(on)}$* area
- High dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested



D²PAK

Application

- Switching applications

Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Figure 1. Internal schematic diagram

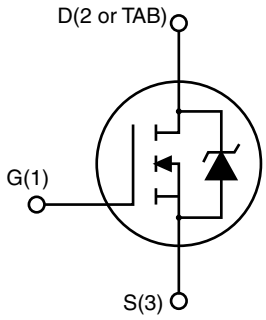


Table 1. Device summary

Order code	Marking	Package	Packaging
STB50N25M5	50N25M5	D²PAK	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	28	A
I_D	Drain current (continuous) at T_C = 100 °C	18	A
I_{DM} (1)	Drain current (pulsed)	112	A
P_{TOT}	Total dissipation at T_C = 25 °C	110	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	9	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	350	mJ
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 28$ A, di/dt $\leq$ 400 A/µs, $V_{Peak} < V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.31	°C/W
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb max	30	°C/W

2 Electrical characteristics

(Tcase =25°C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	250			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 250 V V_{DS} = 250 V, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 14 A		0.065	0.075	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	1700 100 15	-	pF pF pF
$C_{o(er)}$(1)	Equivalent output capacitance energy related	V_{GS} = 0, V_{DS} = 0 to 80% $V_{(BR)DSS}$	-	89	-	pF
$C_{o(tr)}$(2)	Equivalent output capacitance time related	V_{GS} = 0, V_{DS} = 0 to 80% $V_{(BR)DSS}$	-	171	-	pF
R_g	Gate input resistance	f=1 MHz open drain	-	1.8	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 200 V, I_D = 28 A, V_{GS} = 10 V *(see Figure 15)*	-	44 10 23	-	nC nC nC

1. $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}
2. $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 125 V, I_D = 14 A, R_G = 4.7 Ω, V_{GS} = 10 V *(see Figure 14)*	-	16 44 35 20	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		28 112	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 28 A, V_{GS} = 0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 28 A, di/dt = 100 A/µs V_{DD}= 60 V, T_J = 25 °C *(see Figure 16)*	-	174 1.5 18		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 28 A, di/dt = 100 A/µs V_{DD}= 60 V T_J = 150 °C *(see Figure 16)*	-	195 2 20		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

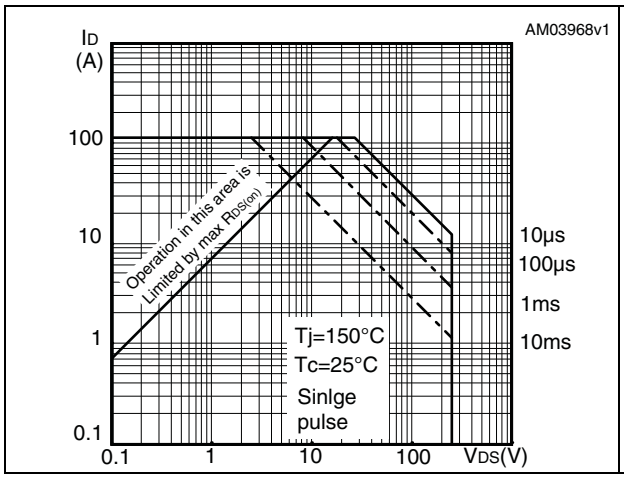


Figure 3. Thermal impedance

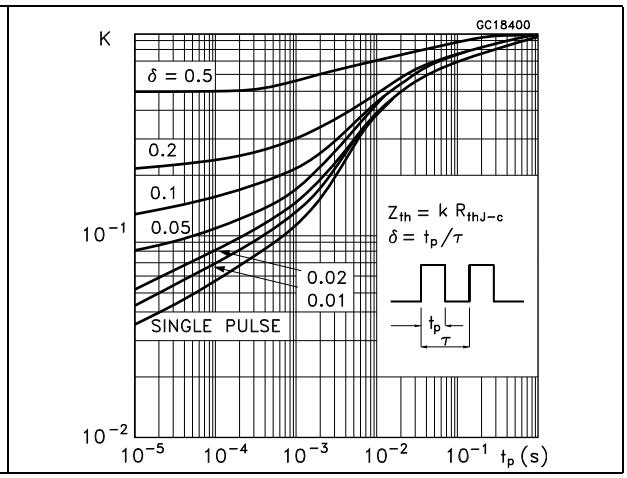


Figure 4. Output characteristics

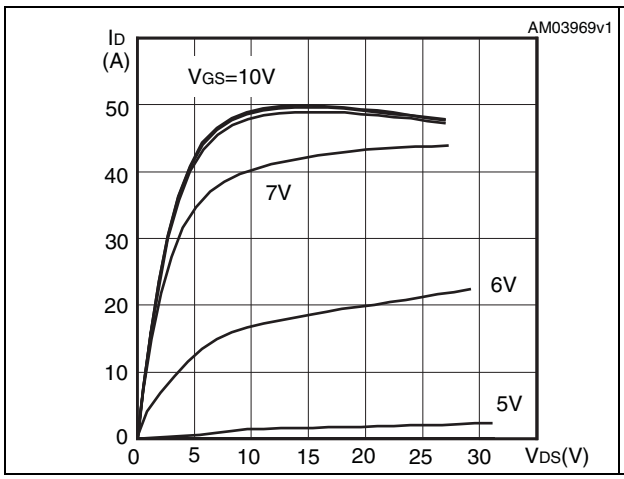


Figure 5. Transfer characteristics

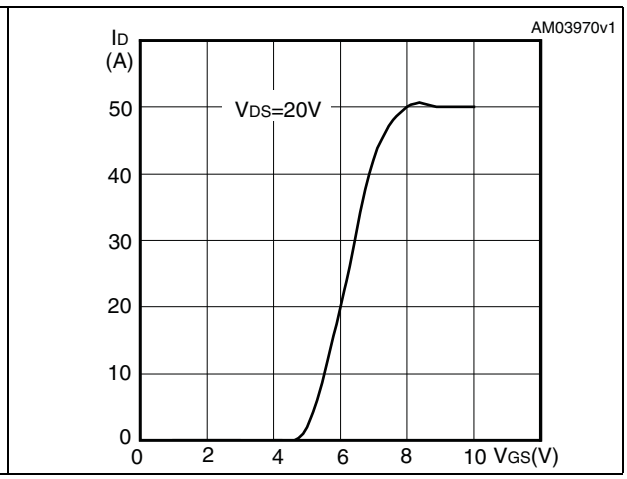


Figure 6. Normalized BV_{DSS} vs temperature

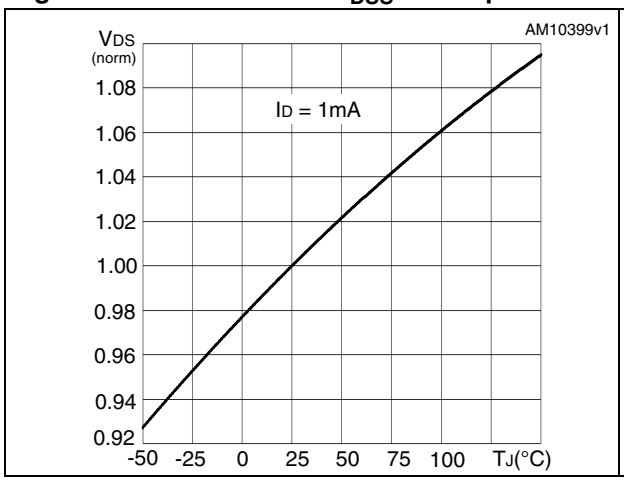


Figure 7. Static drain-source on-resistance

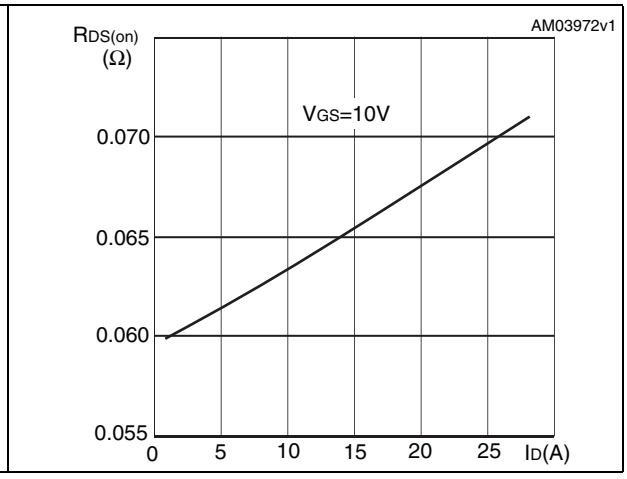


Figure 8. Output capacitance stored energy

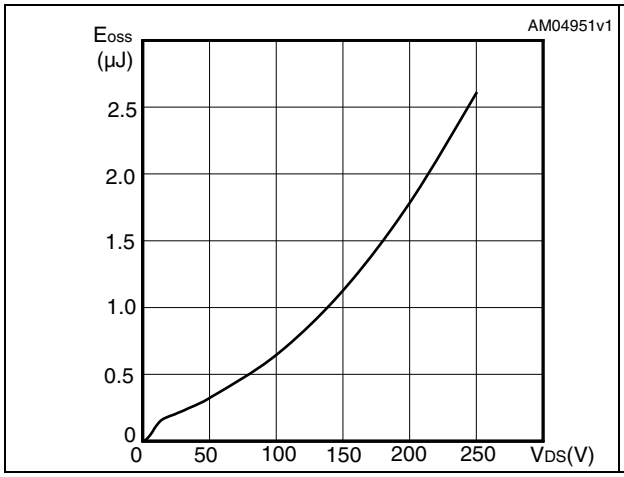


Figure 9. Capacitance variations

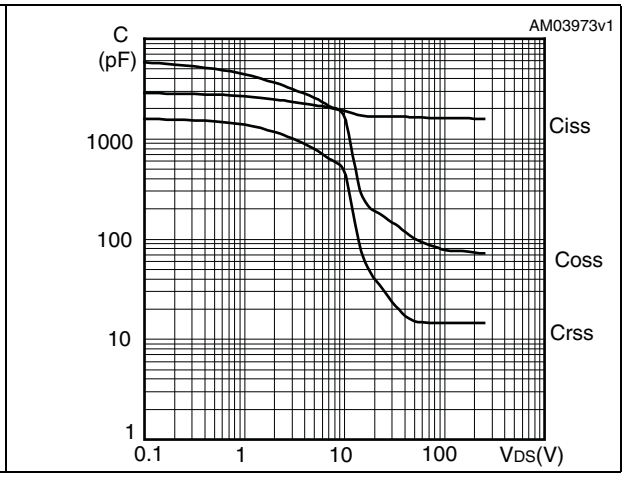


Figure 10. Gate charge vs gate-source voltage

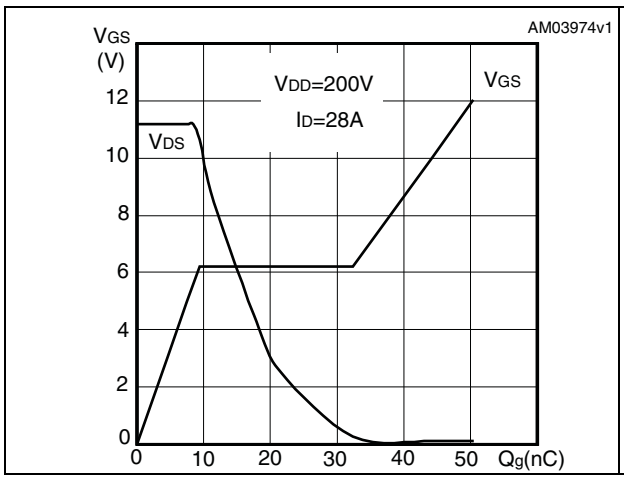


Figure 11. Normalized on-resistance vs temperature

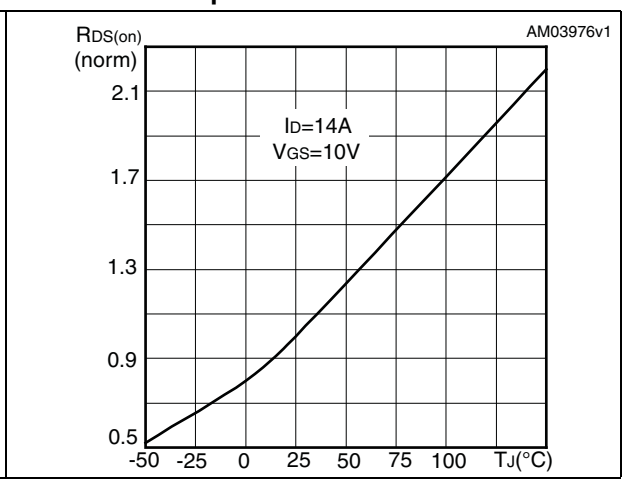


Figure 12. Normalized gate threshold voltage vs temperature

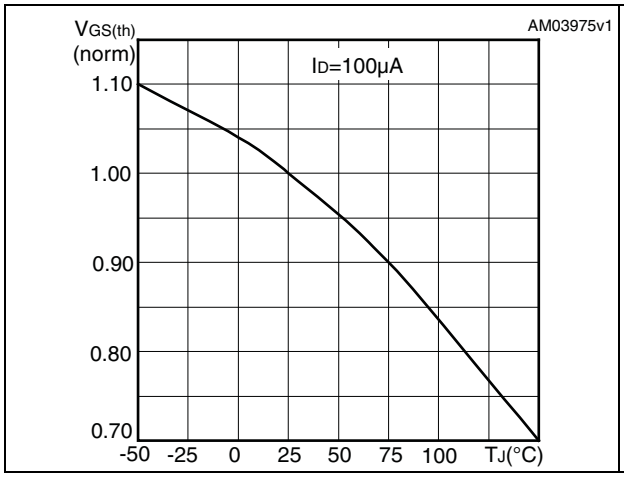
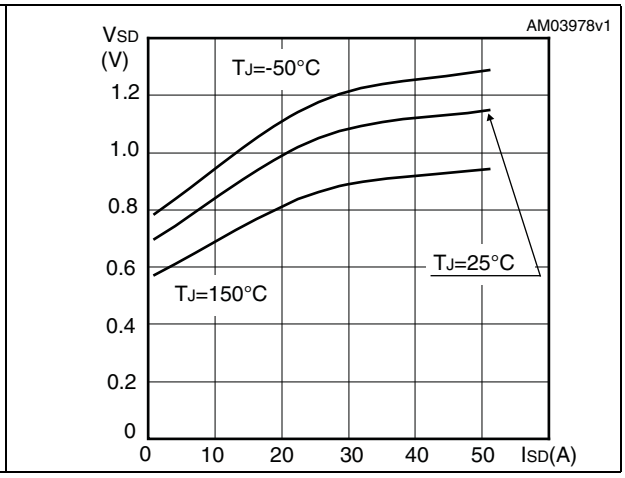


Figure 13. Source-drain diode forward characteristics



3 Test circuits

Figure 14. Switching times test circuit for resistive load

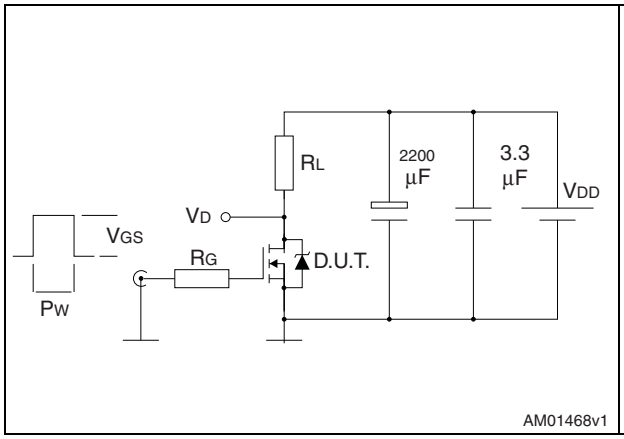


Figure 15. Gate charge test circuit

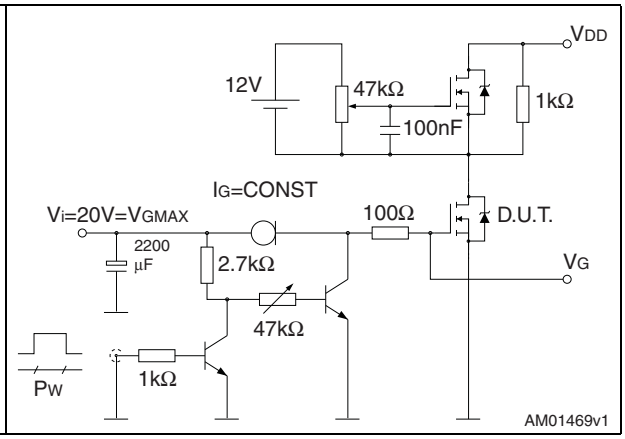


Figure 16. Test circuit for inductive load switching and diode recovery times

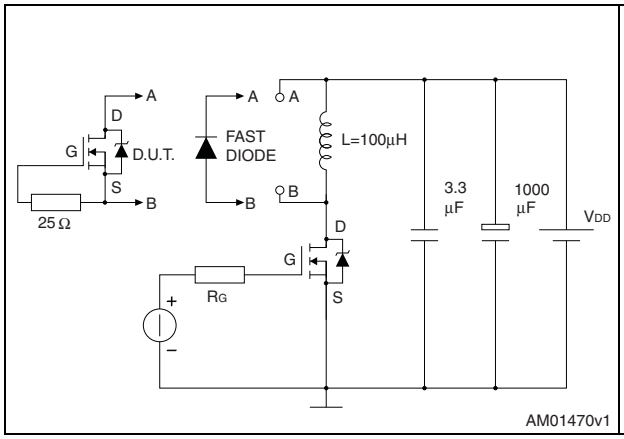


Figure 17. Unclamped inductive load test circuit

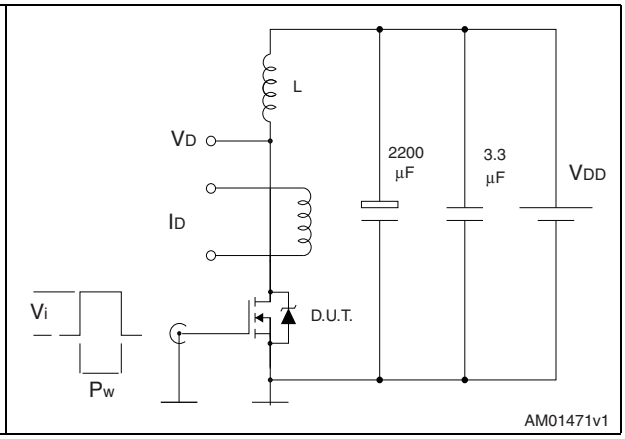


Figure 18. Unclamped inductive waveform

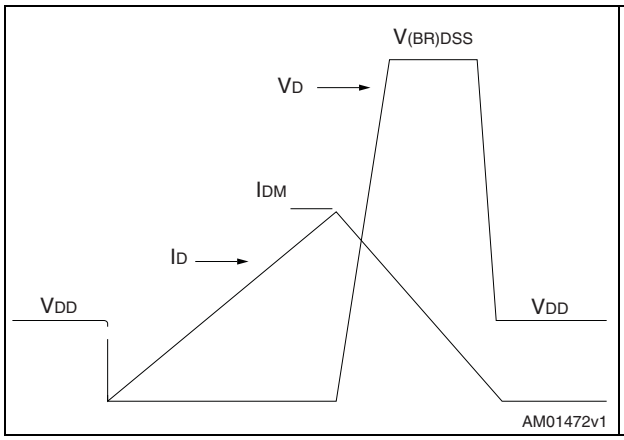
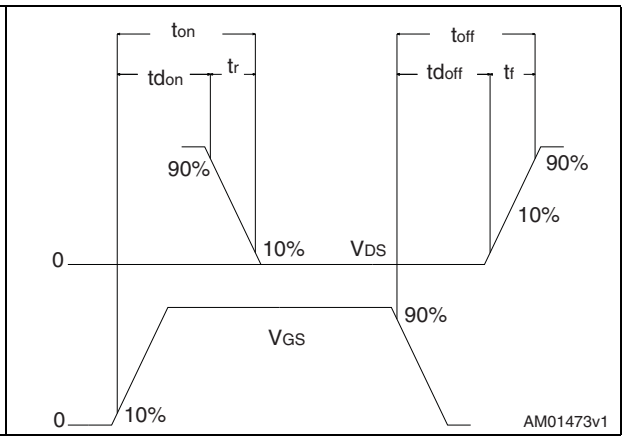


Figure 19. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 20. D²PAK (TO-263) drawing

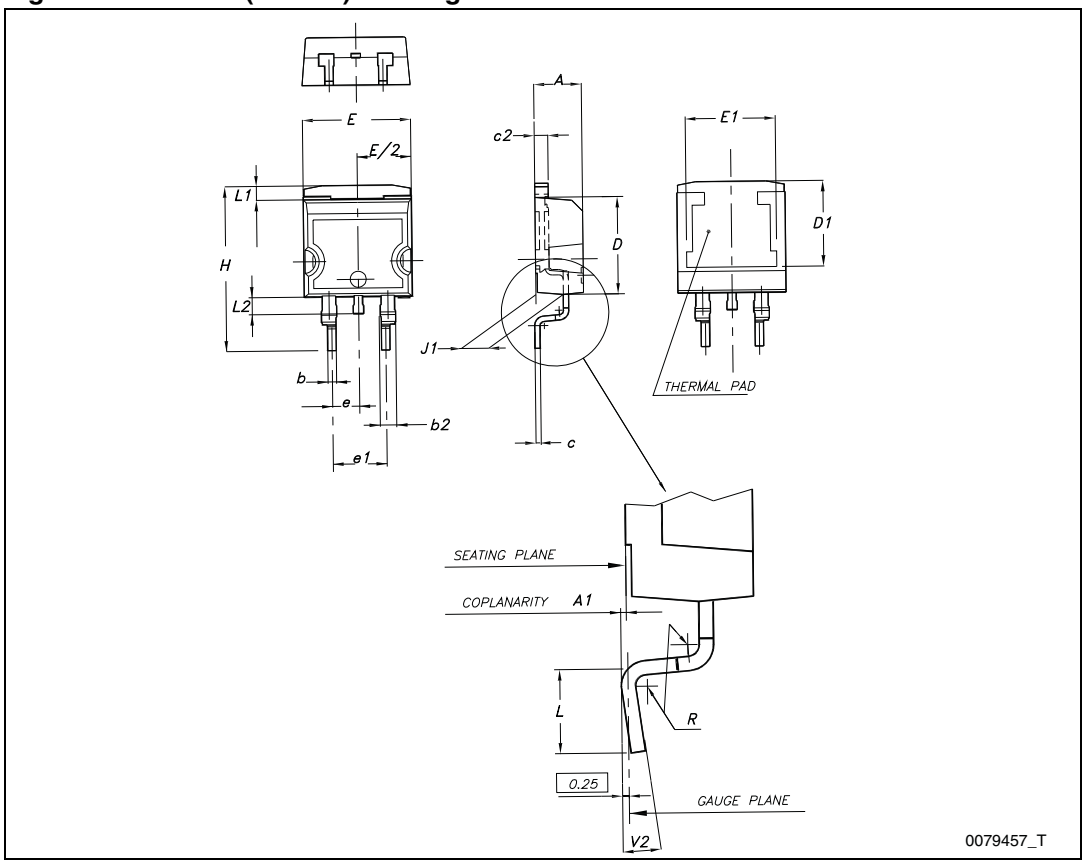
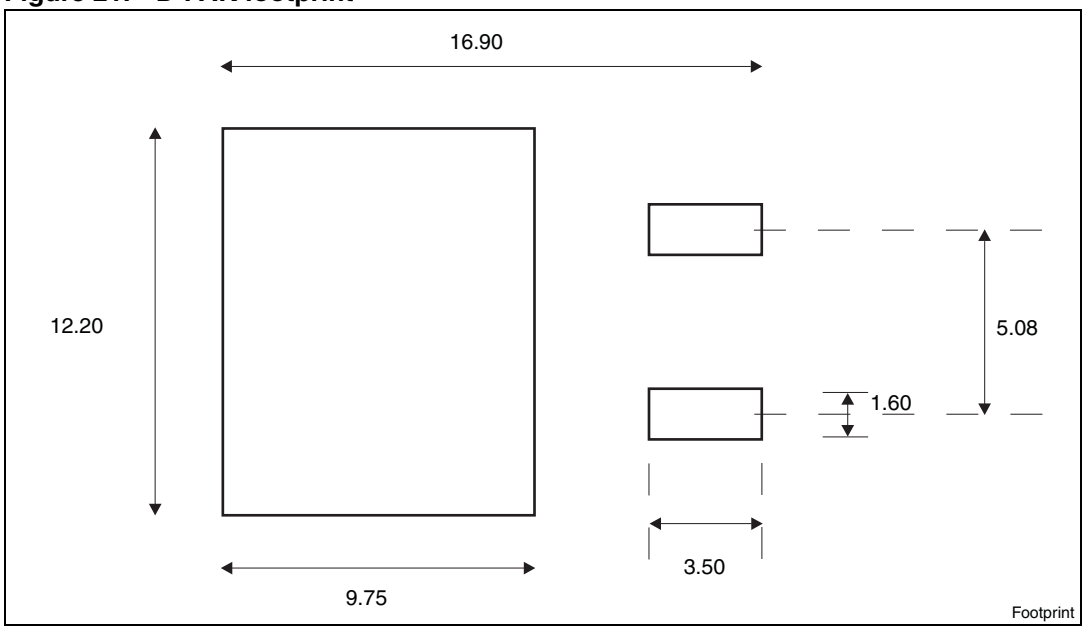


Figure 21. D²PAK footprint[a]



a. All dimensions are in millimeters

5 Packaging mechanical data

Table 9. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 22. Tape for D²PAK (TO-263)

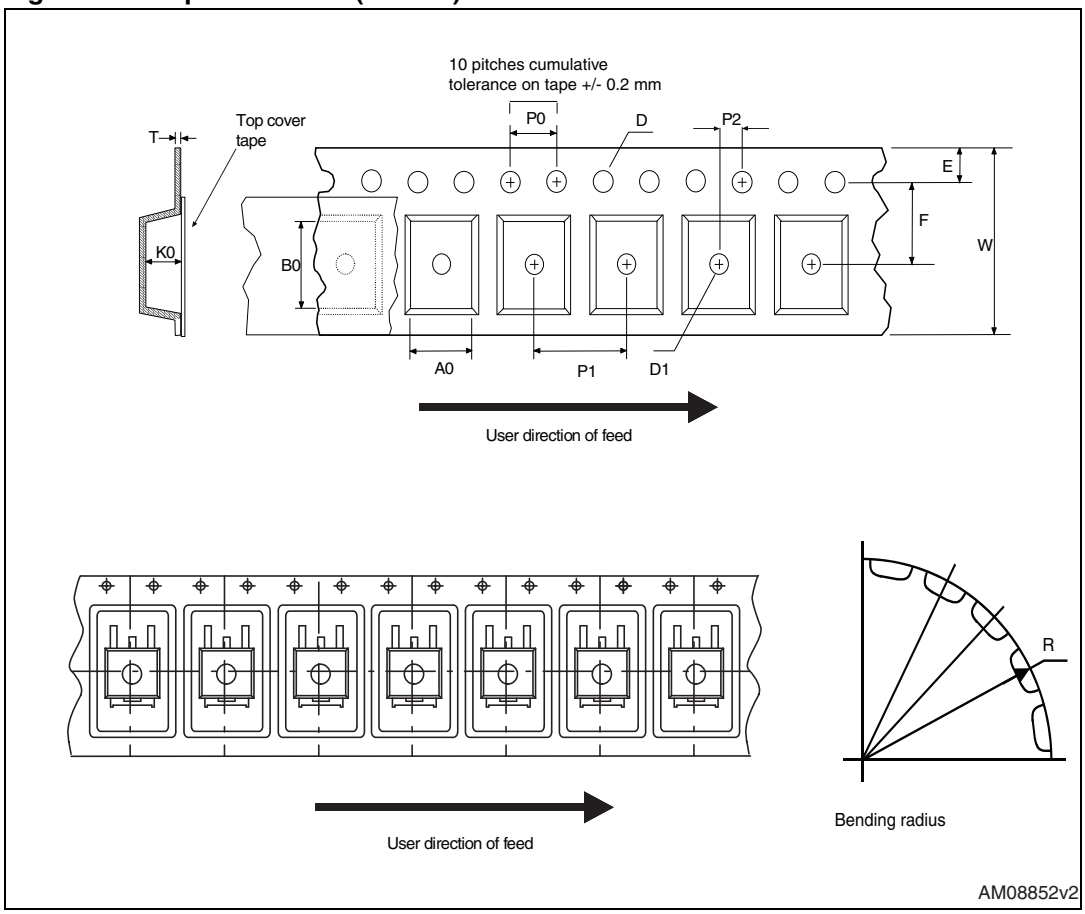
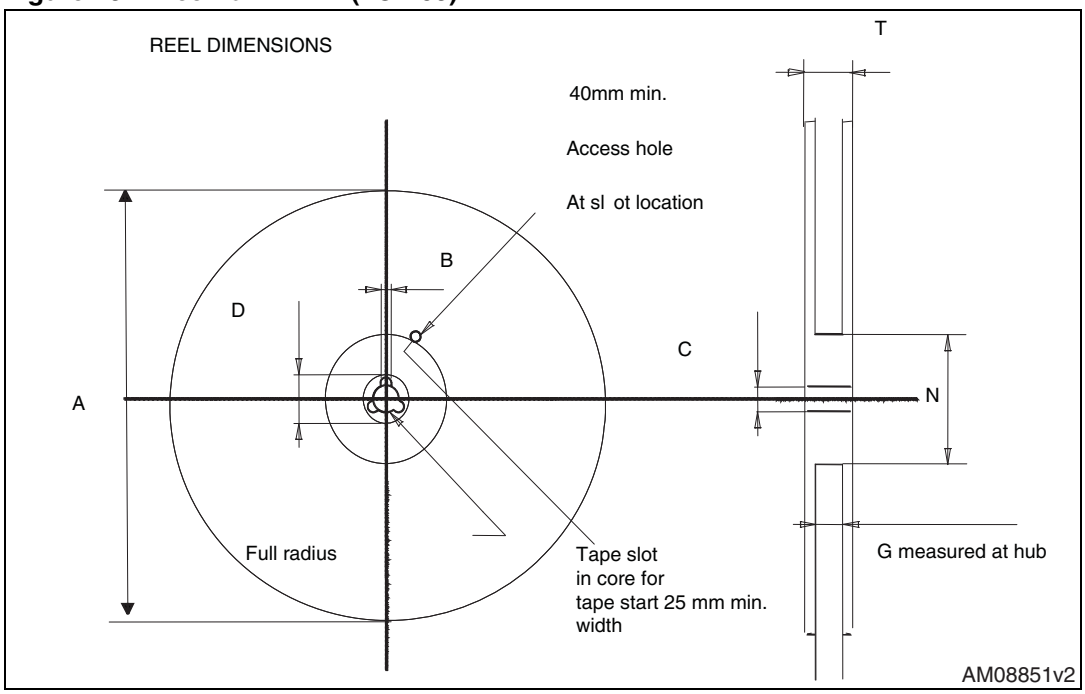


Figure 23. Reel for D²PAK (TO-263)



6 Revision history

Table 10. Document revision history

Date	Revision	Changes
23-Jun-2009	1	First release
15-Mar-2012	2	*Section 4: Package mechanical data* has been updated. Minor text changes.
28-Mar-2012	3	*Figure 7: Static drain-source on-resistance* has been updated.

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